REMARKS

Reconsideration and allowance of this application is respectfully requested. Claims 1-12 are now pending in the present application. Claims 1-12 are rejected. Applicant submits that this application is in condition for allowance and such action is earnestly requested. Each of the Examiner's reasons for rejection is addressed below for the claims that are still pending. Withdrawal of all objections and rejections is respectfully requested for at least the reasons discussed below.

Rejections

35 U.S.C. § 103

The Examiner rejected claims 1-12 under 35 U.S.C. § 103 as being unpatentable over US 2005/0083284 A1 to Huang et al. ("Huang") in view of US 2006/0232351 A1 to Amundson et al. ("Amundson"). Applicant respectfully submits that these claims are patentably distinct over Huang in view of Amundson..

Both Huang and Amundson, alone or in combination, fail to teach or suggest

> *during a pixel writing cycle, applying the select voltage and the data voltages to the select and data lines of the display to produce only three pixel voltage levels 0, +U and –U, having respective duty cycles and controlling the duty cycles of the pixel voltages to determine the gray levels of the pixels, and wherein the average voltage applied to a pixel during the pixel writing cycle is zero.*

as recited in claim 1.

Huang discloses a graphics controller for a color display system having a bistable liquid crystal display (LCD) for displaying a plurality of pixels arranged in a matrix, which includes a memory device and a generating device. In an exemplary case, the bistable LCD is a cholesteric LCD and, preferably, the generating device has a first mode of operation in which the data corresponding to the pixels is generated for each corresponding pixel and a second mode of operation in which no data is generated. The generating device switches from the first operating mode to the second operating mode when all of the status bits for all of the pixels are zeros.

Amundson discloses driving methods and apparatus (i.e., a controller) for driving electro-optic displays, including bistable electro-optic displays. The controller may use a look-up table representing impulses necessary to effect transitions between various gray levels. Some transitions may be DC balanced and may be used for "fine tuning" of applied waveforms to achieve fine control of gray levels without the need for fine voltage control or to reduce the level of DC imbalance.

The present invention relates to a display and a method of driving an active matrix cholesteric liquid crystal display that includes a matrix of data and select lines and an array of pixels connected to the data and select lines through active switching elements, a pixel being capable of producing two or more gray levels, comprising a) providing a select voltage and a plurality of data voltages; and b) during the pixel writing cycle, applying the select voltage and the data voltages to the select and data lines of the display to produce only three pixel voltage levels, 0, +U and –U, having respective duty cycles and controlling the duty cycles of the pixel voltage levels to determine the gray levels of the pixels, and wherein the average voltage applied to a pixel during the pixel writing cycle is zero. The present invention relates to a complete driving scheme wherein only three pixel voltage levels are produced and wherein the average voltage applied during the pixel writing cycle is zero.

As the Examiner has noted, Huang fails to disclose applying the select voltage and the data voltages to the select and data lines of the display to produce only three pixel voltage levels 0, +U and –U. Indeed, Huang discloses using five pixel voltages (40V for ON and 30V for OFF, as well as -40V, -30V, and 0V) and amplitude modulation to determine the gray levels of the pixels. (FIGS. 4, 5a). Thus, Huang fails to disclose a complete driving scheme wherein only three pixel voltage levels are produced and wherein the average voltage applied during the pixel writing cycle is zero.

Amundson does not disclose a complete driving scheme wherein only three pixel voltage levels are produced and wherein the average voltage applied during the pixel writing cycle is zero. The Examiner indicated on page 3 that Amundson discloses

> a bi-stable LCD display (please see abstract), and a driver for applying a select voltage (page 7, paragraph 72, Lines 7-9) and one of a plurality of data voltages to the select and data lines of the display to produce only three pixel voltage levels O, +U and –U (page 7, paragraph 72, 73 where R the reference voltage is zero voltage, page

> 10, paragraph 143) having respective duty cycles and controlling the duty cycles of the pixel voltage levels to determine the gray levels of the pixels (page 7, paragraphs 72, 73, page 10, paragraph 143, please see figures 12A-12E, 25-32, page 42, paragraphs 531,532, page 44, claim text 25) and wherein the average voltage applied to the pixel during the pixel writing cycle is zero (page 10, paragraphs 143, 144, page 19, paragraphs 262, 266, page 6, paragraph 44).

Figs. 12A-12E relate to so-called "non-contiguous" waveforms or "fine-tuning (FT)" waveforms. These FT waveforms may have a zero net impulse and may be used for fine control of gray levels or to reduce the DC imbalance. The FT waveform is separate from the "main" monopolar drive impulse (see page 29, paragraph 0358 "The pulses which may [sic] up such a 'fine tuning' waveform may be separate from the 'major drive' pulses.") These FT waveforms alone do not constitute a complete drive scheme (see page 29, paragraphs 0359-0362). While an individual FT waveform may have a zero net impulse, the combination of that FT waveform and the major, or main drive impulse may not have a zero net impulse.

Figs. 25-32 relate to a so-called "DC balanced addressing" method. DC balance means that "all full-circuit gray level sequences (sequences that begin and end with the same gray level), have zero net impulse." (page 31, paragraph 0415) Amundson also discloses DC balanced transitions, where the transition from one gray level to another has zero net impulse. A DC imbalanced transition is one where the transition has a non-zero net impulse. Three types of DC balanced transitions are described and shown in Figs. 25-32. These DC balanced transitions do not constitute a complete driving scheme. Indeed, Amundson specifically discloses that "Finally, DC balanced transitions can be combined with DC imbalanced transitions to form a complete drive scheme." (page 36, paragraph 0462). Indeed, the waveform shown in FIG. 32 is not DC balanced, and only the "NC" (no change in gray level) transitions in Table 11 are DC balanced. Amundson further discloses that "[i]t is desirable to maximize the number of transitions which are DC balanced. However, depending on the specific electro-optic medium being used, it may be difficult to DC balance transitions involving transitions to or from extreme gray levels, for example to or from black and white, gray levels 1 and 4 respectively." (page 37, paragraph 0463) Thus, Amundson does not teach a complete driving scheme wherein only three pixel voltage levels are produced and wherein the

average voltage applied during the pixel writing cycle is zero because the driving schemes include DC imbalanced transitions where the average voltage applied is not zero for each DC imbalanced transition.

Neither Huang nor Amundson, alone or in combination, discloses a complete driving scheme wherein only three pixel voltage levels are produced and wherein the average voltage applied during the pixel writing cycle is zero. Thus, claim 1 is patentable over Huang and Amundson. Similarly, claim 7 is patentable over Huang and Amundson for the same reasons as above.

Claims 2-6, which depend on claim 1, and claims 8-12, which depend on claim 7, are similarly patentable over Huang and Amundson, at least for the same reasons as above.

CONCLUSION

Based on the foregoing, Applicant respectfully submits that all pending claims in the present application are in condition for allowance and respectfully requests withdrawal of the outstanding rejection the issuance of a formal Notice of Allowance at an early date.

Applicant thanks the Examiner for carefully examining the present application and considering this response and if a telephone conference would facilitate the prosecution of this application, the Examiner is invited to contact Applicant's attorney at the number listed below.

Respectfully submitted,

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(Date)

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